CLAIMS

___ There are no amendments to the claims.

_X_ A complete listing of all claims ever present in this case in ascending order with status identifier is presented in a separate section.

COMPLETE LISTING OF CLAIMS

IN ASCENDING ORDER WITH STATUS INDICATOR

1-55. (Canceled)

56-57. (Canceled)

58. (Previously Presented) A latching circuit comprising:

a first p-channel transistor having a first drain, a first gate, and a first source, said first drain operatively connected to a source of a first supply voltage;

second and third p-channel transistors having respective second and third drains, second and third gates, and second and third sources, said second and third drains mutually operatively connected to said first source;

first and second n-channel transistors having respective fourth and fifth drains, fourth and fifth gates, and fourth and fifth sources, said fourth drain operatively connected to said second and third sources, said fourth source operatively connected to said fifth drain, said fifth source operatively connected to a source of a second ground voltage, said fourth gate operatively connected to said second gate;

an inverter having an input operatively connected to said fourth drain and an output operatively connected to said third and fifth gates; and

a third n-channel transistor having a sixth drain, a sixth gate, and a sixth source, said sixth source operatively connected to said input of said inverter, said third n-channel transistor adapted to provide a conductive path between said sixth drain and said sixth source in response to a signal above a threshold magnitude applied at said sixth gate, wherein said third n-channel transistor is adapted to have said threshold magnitude adjusted in response to an electrical signal applied between said sixth drain and said sixth gate.

59. (Previously Presented) A method of recording an identity of a memory device comprising:

applying a programming voltage between a respective drain and gate of a transistor disposed within said memory device, and said transistor having a gate threshold adapted to transition from a first value to a second value in response to said programming voltage, whereby said first value corresponds to a first identity and said second value corresponds to a second identity.

60. (Previously Presented) A method of reading an identity of a memory device comprising:

applying a read voltage to a gate of a transistor having a programmed gate threshold voltage for a time interval, said transistor disposed within said memory device;

reading a conductivity state of said transistor during said time interval; and

perceiving an identity of said memory device according to said conductivity state.

61. (Previously Presented) A method of remapping a defective memory cell address comprising:

applying a programming voltage between a gate and a source of a programmable transistor and thereby changing a gate threshold of said transistor to correspond to a programmed state;

applying a read signal voltage to said gate of said transistor, causing said transistor to output a signal corresponding to said programmed state;

communicating said output signal of said transistor to an input of an address decoder; and

changing an output of said address decoder in response to said communicated signal so as to select a non-defective memory cell.

62. (New) A method of forming a logical data storage device comprising:

coupling a gate of a programmable threshold transistor to a first voltage node, said voltage node adapted to receive an electrical potential between a programmed gate threshold voltage and an unprogrammed gate threshold voltage of said programmable threshold transistor; and

switchingly coupling an input of a latching circuit through said programmable threshold transistor to a second voltage node, said second voltage node adapted to be coupled to a source of substantially constant electrical potential.

63. (New) A method of forming a logical data storage device as defined in claim 62, wherein said source of substantially constant electrical potential comprises a ground node.

64. (New) A method of forming a logical data state storage device comprising:

coupling a supply voltage node to a first source of a first field effect transistor, said first field effect transistor including a first drain;

mutually coupling said first drain to respective second and third sources of a second and a third field effect transistor, said second and third field effect transistors having respective second and third drains;

mutually coupling said second and third drains to one another and to an input of an inverter circuit and a fourth drain of a fourth field effect transistor, said fourth field effect transistor having a fourth source;

coupling said fourth source to a fifth drain of a fifth field effect transistor, said fifth field effect transistor having a fifth source;

coupling said fifth source to a ground node;

coupling a first gate of said first field effect transistor to a first input node;

mutually coupling a second gate of said second field effect transistor and a fourth gate of said fourth field effect transistor to a second input node;

mutually coupling a third gate of said third field effect transistor and a fifth gate of said fifth field effect transistor to an output of said inverter circuit and a first output node;

coupling said input of said inverter circuit to a sixth source of a sixth field effect transistor;

coupling a sixth drain of said sixth field effect transistor to a ground node; and

coupling a sixth gate of said sixth field effect transistor to a third input node.

65. (New) A bi-stable logic device comprising:

a switching device adapted to receive a gate signal during a first time interval, said gate signal having a magnitude within a range between a first threshold magnitude of said switching device and a second threshold magnitude of said switching device; and

a latching device adapted to receive an output from said switching device and output a latch output signal during a second time interval, said latch output signal related to a state of said switching device during said first time interval.

66. (New) A bi-stable logic device as defined in claim 65 wherein said switching device comprises a field effect transistor, said first threshold magnitude includes a programmed gate threshold voltage of said field effect transistor, said second threshold magnitude includes an un-programmed gate threshold voltage of said field effect transistor, and said magnitude of said gate signal defines an electrical potential applied to a gate of said field effect transistor.

67. (New) A bi-stable logic device as defined in claim 66 wherein said field effect transistor is an N-channel field effect transistor and said latching device comprises an

inverter circuit having an input node coupled to a source terminal of said field effect transistor.

68. (New) A bi-stable logic device as defined in claim 67 wherein said field effect transistor is a P-channel field effect transistor and said latching device comprises an inverter circuit having an input node coupled to a drain terminal of said field effect transistor.